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Fuzzy Logic Controller for An Asymmetric Multilevel Inverter in Railway EMUs with Different Motor Loading Effects

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Abstract

This study specially focused on Railway Electrical-Multiple-Units (E-M-Us) and demonstrate the implementation of 9-level Asymmetric-Cascaded H-bridge (AC-H-B) Multilevel Inverter (MLI) controlled with Fuzzy-Logic-Controller (F-L-C) in order to boost the class of output waveforms with the elimination of major harmonic contents in the output result. As the operation of railway EMUs system needs higher power as well as voltage. Thus it is an excellent choice to utilize Asymmetric Multi-level Inverter instead of Classical Inverter. An Asymmetric MLI which is controlled here utilizes 2-H-bridge modal with un-equal D-C supplies and it can be able to make multi-level sinusoidal waveform at the output for 3-phase Inductor Motor. Various parameters of motor with different loading condition have been studied. Here an Asymmetric MLI utilizes limited semi-conductor IGBT switches and D-C voltage supply. Therefore financial spending and size of the railway EMU system will be compressed. So as efficiency of system will improve. Prototypical Simulation has been performed by MATLAB/simulink software in order to verify the operation of an Asymmetric MLI based EMU system.

Keywords: Asymmetric Multi-level Inverter, Electric-Multiple-Units, Fuzzy-Logic-Controller, Super Imposed Carrier Pulse-width modulation, Total Harmonic Distortion (THD).

Introduction

The progress of semi-conductor type of electronic components for the duration of 19th centennial trigged the concern regarding exchange of electrical power for variety of appliance. Modernity in societies is looking towards an escalating requirement of electric power, so research for electric power converter equipments become significantly important. Semi-conductor based inverters are extensively adopted for efficient controlling, distributing and economically transfer of electric power [1-2].

Electrical conversion devices have been adopted in variety of appliance. Like domestic equipments such as adapter of phones, television, computers, luminous equipments and industrial equipments like steel mills, railway traction as well as distribution along with transmission network. Railway traction system uses electric power conversion equipments with high power rating [3]. Commonly these systems use conventional equipments due to its wide applications. As significance of such a wide application scope and in order not to overuse valuable resources along with reduction in the impact of human activities on environment, power-converter systems have to be required. There are so many developments have been done so far in order to get higher effectiveness of semi-conductor converter devices.

When look for the alternatives, wide variety of Multi-level Inverter (MLI) [4-5] topologies have been suggested, which can produces a fruitful voltage waveforms. In mentioned scenario, sinusoidal waveform can be realized, if the required quantities of steps are to be large enough. As per efficiency point of view, this piece of evidence realized through an extremely low valued frequency of switching per switches, thus building this MLI family extremely eye-catching [6-8]. On the other hand, there have been numerous causes why these MLI configurations not subjugated in the electrical inverter equipments, apart from their profitable characteristics. When deep analysis has been taken for all the active used configurations, it is clear that structural complication would extensively influence the dependability of these inverters.

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The MLI family unit started a new field of investigation for inverters with rating of medium voltages and higher powers. Amongst various MLI configurations, the cascaded H-bridge (C-H-B) has been paying special attention due to its modular type structure, so as to have better fault tolerance. Therefore, C-H-B MLI has been acknowledged in renewable energy based systems, reactive power compensation (STATCOMs) and drive applications. Comprehensive studies have been performed for different topologies of MLIs [7-9]. It is considered as highly competitive MLI topologies mainly applied for medium voltages and large-powers. Modulation has a deep impact on the performance of an MLI. The well-liked modulation method discussed in the literature for MLIs are multicarrier-based PWM [10-11], multilevel selective harmonic elimination (SHE) [12-14] and multilevel space-vector PWM (SVM) [15]. Every technique has its diverse advantages and limitations. As a result, the selection of the modulation method depends on the configurations and applications of an MLI. However there are many questions still unanswered with reference to the properties and performance of these MLIs. MLIs are having plentiful requirement in areas like as grid connected photovoltaic systems, industrial drives, railway traction drives and electric vehicles. The present work of this article delivers an idea to utilise an asymmetric MLI topology for railway EMUs and fuzzy logic control strategy which may be suitable for railway traction systems.

In this manuscript, an asymmetric C-H-B MLI for railway EMUs has been adopted. Two D-C voltage source with 3:1 ratio are needed per phase for 9-level of output. In the analysed asymmetric MLI, the number of components utilized and harmonic contents in the voltage waveform are reduced as compared with the conventional inverters. Theoretical study and prototypical simulations results shows the confirmation of the proposed 9-level MLI based EMU system. As a final point, the operation of 9-level MLI based EMU system in producing all predictable levels of voltage with a 9-step MLI is justified by simulation in MATLAB/Simulink software.

The proposed paper is structured as follows: Section II discusses the asymmetric MLI topologies, Section III discusses the proposed EMU power circuit with 9-level MLI, Section IV demonstrates the loss calculation, and Section V discusses comparison of the proposed modular topology with the latest and old conventional topologies. Section VI presents simulation results, followed by conclusion in the Section VII.

Asymmetric MLI Topologies

The key idea of this asymmetric MLI topology is to make 1:3 ratio between its input D-C voltage supply in order to quantize the input voltage for MLI.

Building Block Modules

Fig. 1 shows an H-bridge circuit which consists of four semiconductor switches with four anti-parallel diodes. *S*1 to *S*4 are the IGBT switches. Where, *S*1, *S*3 are used for positive level output and *S*2, *S*4 are used for negative level output. A building block module is capable to generate higher levels with cascading of additional such modules

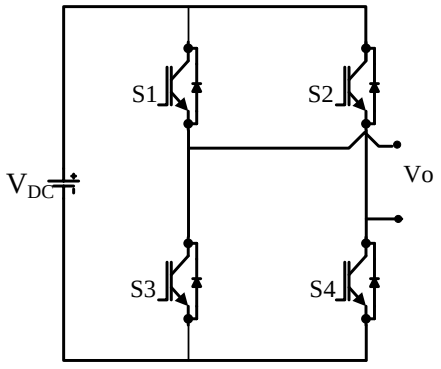

Fig.1. Basic Building Block H-bridge Module

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Asymmetric MLI Structure

Fig. 2 depicted a multi-structured asymmetric MLI comprised of two building block modules of Fig. 1. In Fig. 2, an asymmetric modular topology is analysed for a 9-level MLI. As given in the Fig. 2, analysed asymmetric modular topology is accumulated by adding cascaded connection of two H-bridges with their input voltage supply ratios of 3:1.

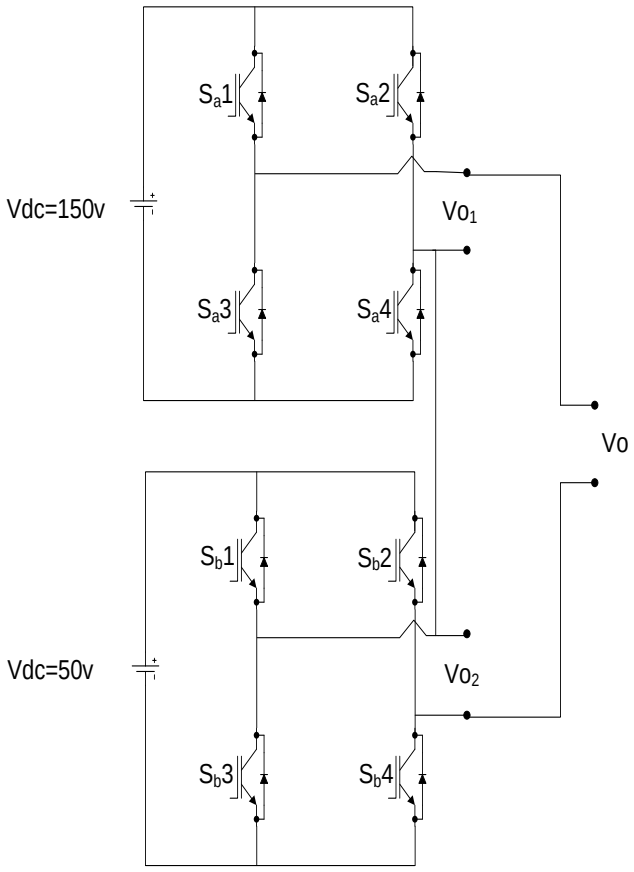

Fig.2. Asymmetric Cascaded H-bridge MLI

The proposed asymmetric MLIs are consists of eight IGBT switches (S_{a1}, S_{a2}, S_{a3}, S_{a4}, S_{b1}, S_{b2}, S_{b3} are S_{b4}) and two D-C voltage sources (*Vdc1 and Vdc2*). In this paper, this topology is called as **Asymmetric Cascaded H-bridge (AC-H-B)** MLI. As shown in Fig. 2, the simultaneous switch-on of ((S_{a1}, S_{a3} & S_{a2}, S_{a4}) and (S_{b1}, S_{b3} & S_{b2}, S_{b4})) makes short-circuit in the structure. As a result, simultaneous switching-on of the above discussed IGBT switches have to be eliminated. Table I shows the voltage output of analysed asymmetric MLI for dissimilar switching states. In table I, 0 and 1 designate as OFF and ON switching states, correspondingly.

When the D-C supply voltages are alike, the quantity of voltage steps lower to five. Thus, the D-C supply voltages have to be different to produce additional steps without escalating the quantity of IGBT switches and D-C supply voltage. Taking into consideration table I, to create all 9- steps in the analysed asymmetric modular topology depicted in the Fig. 2, the values of V_{DC1} and V_{DC2} should be consider 3*pu* and 1*pu*, correspondingly.

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TABLE I. Swiching Combination for 9-level ACHB MLI

Figure 1. S_{a1}	Figure 2. S_{a2}	Figure 3. S_{a3}	Figure 4. S_{a4}	Figure 5. S_{b1}	Figure 6. S_{b2}	Figure 7. S_{b3}	Figure 8. S_{b4}	Figure 9. V_{DC}
Figure 10. 1	Figure 11. 0	Figure 12. 1	Figure 13. 0	Figure 14. 1	Figure 15. 0	Figure 16. 1	Figure 17. 0	Figure 18. $+4V_{DC}$
Figure 19. 0	Figure 20. 0	Figure 21. 0	Figure 22. 0	Figure 23. 1	Figure 24. 0	Figure 25. 1	Figure 26. 0	Figure 27. $+3V_{DC}$
Figure 28. 0	Figure 29. 1	Figure 30. 0	Figure 31. 1	Figure 32. 1	Figure 33. 0	Figure 34. 1	Figure 35. 0	Figure 36. $+2V_{DC}$
Figure 37. 1	Figure 38. 0	Figure 39. 1	Figure 40. 0	Figure 41. 0	Figure 42. 0	Figure 43. 0	Figure 44. 0	Figure 45. $+1V_{DC}$
Figure 46. 0	Figure 47. 0	Figure 48. 0	Figure 49. 0	Figure 50. 0	Figure 51. 0	Figure 52. 0	Figure 53. 0	Figure 54. 0
Figure 55. 0	Figure 56. 1	Figure 57. 0	Figure 58. 1	Figure 59. 0	Figure 60. 0	Figure 61. 0	Figure 62. 0	Figure 63. $-1V_{DC}$
Figure 64. 1	Figure 65. 0	Figure 66. 1	Figure 67. 0	Figure 68. 0	Figure 69. 1	Figure 70. 0	Figure 71. 1	Figure 72. $-2V_{DC}$
Figure 73. 0	Figure 74. 0	Figure 75. 0	Figure 76. 0	Figure 77. 0	Figure 78. 1	Figure 79. 0	Figure 80. 1	Figure 81. $-3V_{DC}$
Figure 82. 0	Figure 83. 1	Figure 84. 0	Figure 85. 1	Figure 86. 0	Figure 87. 1	Figure 88. 0	Figure 89. 1	Figure 90. $-4V_{DC}$

EMU Circuit Structure

The EMU circuit of railways is appropriate for working under 1500V DC or 25 KV AC dual voltage systems. EMU circuit has following key components: Pantograph, Surge-Arrestor, Voltage sensing device, AC-DC change-over switch, Vacuum circuit-breaker, High speed circuit-breaker, Main traction transformer, D-C link capacitors and Converters (4 quadrant chopper, brake chopper and PWM inverter). The general diagram of EMU circuit is depicted in fig. 3. As shown from figure is that EMU circuit is such a vast system and it has reduced efficiency because of the use of conventional equipments.

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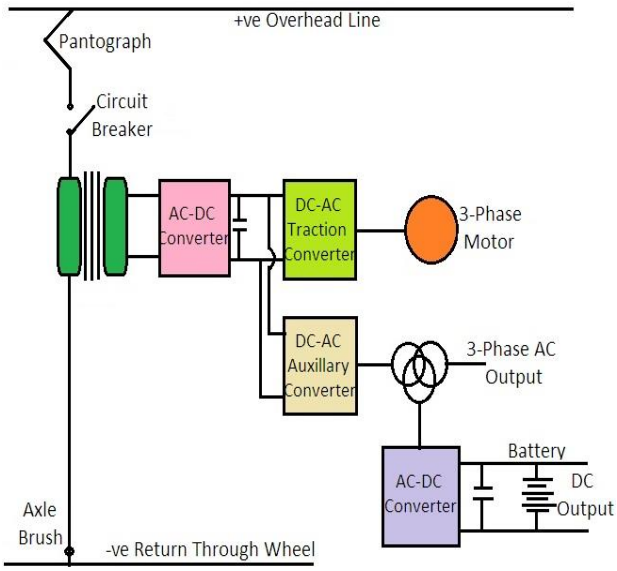

Fig.3. Generalised block drawing of EMU power circuit

EMU circuit with Conventional inverter

Inverter device utilized in EMUs of Railway is conventional one, which is 3-phase conventional inverter. As shown from fig. 4. EMU circuit is consists of supply of 25kv single phase AC fed to a transformer with dual secondary winding. Output supply of transformer is goes to AC-DC converter then fed to D-C link. D-C link consists of capacitors with inductors in series as well as parallel respectively. Output of D-C link fed to DC-AC converter, which is 3-phase inverter. Output of conventional inverter is goes via LC filter for making harmonic free supply to load.

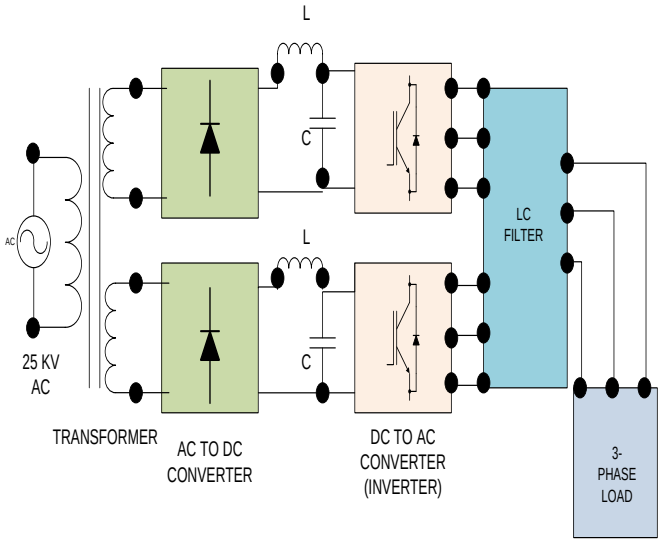

Fig.4. EMU power circuit with conventional inverter

EMU circuit with ACHB multilevel inverter

Multilevel inverter can be utilized in EMUs of railway. Three single-phase MLIs are utilized here for making 3-phase MLI as depicted in fig. 5. Proposed EMU circuit gets supply of 25kv single phase AC fed to a transformer with dual secondary winding. Output supply of transformer is goes to AC-DC converter then fed to D-C link. D-C link consists of inductors and capacitors, series and parallel respectively. Output of D-C link fed to DC-AC converters, which are three single-phase MLIs. Topology used in MLI is ACHB. Output of multilevel inverter is directly goes to load without using LC filter for making harmonic free supply to load.

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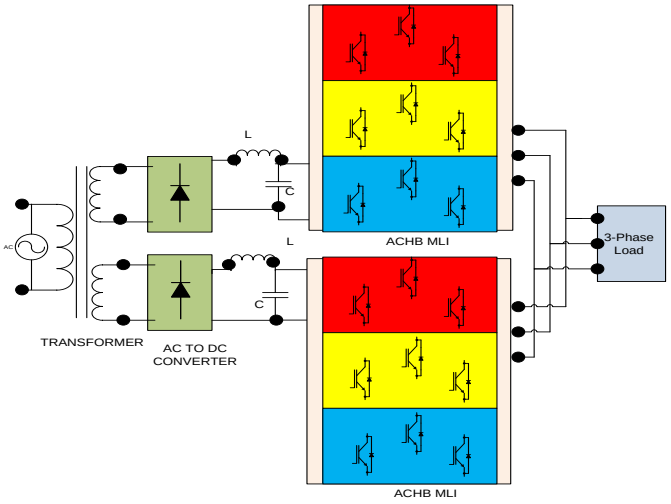

Fig.5. EMU circuit uses ACHB-MLI

Fuzzy Logic based Controlling of EMU Circuit

Fuzzy Logic Controller

Fuzzy logic based controller implementing methodology which is knowledge based and it utilizes experiences of fuzzy logic operators. Non-linear based systems are far more useful for this type of controller. Fuzzy logic based controller is implemented here in this MLI based EMU circuit configuration for producing desired quality output and least amount harmonic contents. In FLC, controlling action is implemented through the consideration of easy language based rules.

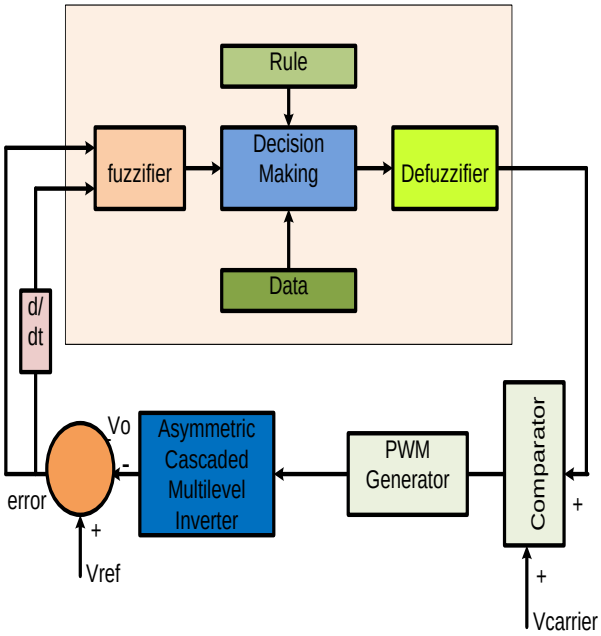

Fig.6. Scheme of FLC for ACHB-MLI

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1)FLC is divided into five sub-parts as shown in Fig. 6. These sub-parts are as follows: Fuzzifier, Defuzzifier, rule, Decision Making and Data. As per above given scheme, Table II describes rule base for FLC.

2)

3)Table-II: Inference Rules for FLC

e/d/de	N-B	N-M	N-S	Z	P-S	P-M	P-B
N-B	N-B	N-B	N-B	N-M	N-M	N-S	Z
N-M	N-B	N-B	N-M	N-M	N-S	Z	P-S
N-S	N-B	N-M	N-M	N-S	Z	P-S	P-M
Z	N-M	N-M	N-S	Z	P-S	P-M	P-M
P-S	N-M	N-S	Z	P-S	P-M	P-M	P-B
P-M	N-S	Z	P-S	P-M	P-M	P-B	P-B
P-B	Z	P-S	P-M	P-M	P-B	P-B	P-B

EMU Circuit with FLC based ACHB MLI

This manuscript shows the prospective of an EMU circuit governed by the fuzzy logic based controller using ACHB MLI. As shown in Fig. 6, scheme of FLC with ACHB MLI consists of FLC model and ACHB MLI model which is a symbol for entire EMU circuit, PWM generator, summer and comparator. Its operation is initiated with the utilization of signal generator of reference voltage which has striking frequency, amplitude and phase. Here FLC has signal of feedback and its output signal is continuous waveform send to ACHB MLI model. These are functions of condition based statement creating discrete signals for gate pulse of the ACHB MLI.

The variable at the input of FLC:

- The differentiation for signals of reference and actual output as $AV_{diff} = V_{Ref} - V_o$.

The signal of output for FLC is send to MLI control driver circuit for gating signal. Here are 11 different states for the output of FLC. A data base was generated firstly during the design procedure of FLC, (i.e. rules of fuzzy logic, behaviour, articulated through statements and situations). Starting since situation "TRUE" (i.e., condition has established), error signal formed by the formation of set of rules. Afterwards situations were created by getting variable reactions. Type and number of membership-functions (MFs) represents a solution for the FLC. Data allocation of input is responsible for Shape of MFs and the time of implementation and accurateness of tracking are influenced by its shape. Denotation "N-B," "N-M," "N-S," "ZE," "P-S," "P-M," and "P-B" are adopted for error signal =AVdiff and for other variable also. Here: "N-B" = negative-big, "N-M" = negative-medium, "N-S" = negative-small, "ZE" = zero, and so others. In this research article, the type and quantity of the FLC rules were determined according to study prepared by changing the type and number of rules.

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In this manuscript, simulation diagram is designed with MATLAB/simulink software. Fig. 6 depicted the configuration of closed loop control circuit for 9-level ACHB MLI. Feedback of output signal has been send to summer for comparing the output signal along with reference signal in order to obtain error signal. Here 2-input signals are used in FLC, one is error signal and other is derivative of error signal. The task of the FLC is to translate the observed inputs which are crisp in nature into sets of fuzzy by process of fuzzification, afterward the sets of fuzzy is processed with the help of fuzzy rules and fuzzy inference system help to perform evaluation mechanism. A set of fuzzy is again produced as an Output from the fuzzy inference system, afterwards by the process of defuzzification these are again transformed to output signal which is crisp in nature. The above created output is compared along with carrier wave which is triangular in nature to create gate pulses for control driver circuit of the 9-level ACHB MLI.

Simulation Results

The simulation results of EMU circuit with classical inverter and ACHB multilevel inverter is evaluate by means of MATLAB/Simulink software. The PWM scheme is in demand for pulse generation. The IGBT type switches are desired for its fast switching ability and power handling capability. 3-Phase induction motor load is used for the simulation purpose. Control signals are generated with the use of PWM scheme.

The simulation circuit of MATLAB simulink for analyzed ACHB MLI consists of 8 IGBT type switches for generation of 9-levels as depicted in figure 5. The waveform of output voltage of EMU circuit with classical inverter is depicted in figure 7. Results of harmonic investigation of output voltage of EMU circuit with classical inverter are depicted in Fig 9. The waveform of output voltage of the EMU circuit with ACHB MLI is depicted in the figure 8. Results of harmonic analysis of output voltage of EMU circuit with ACHB MLI have been shown in Fig.10. In the Fig.10 THD quantity has quite low value for lower and odd harmonic number with the implementation of sinusoidal P-W-M methods. P-W-M controlling method is quite used for any number of levels. As compare to other controlling methods, it has complication level is low. Fig.11 to Fig.14 depicted various parameters (rotor current, stator current, speed of motor and electrical torque) of motor load for 9- level ACMLI based EMU circuit. In the Fig.11 to Fig.14 various motor parameters has been described, at the external load torque value of 10Nm, all the motor parameter has excellent output. Rotor current is having zero value after steady state, while stator current has minimum amount of value after steady state. From the results of motor load, it is concludes that as the applied torque increases time to achieve steady state increases. The analyzed method produces gating signals and fed separately these signals at particular IGBTs. The results of simulation circuit are verified that the configuration circuit is properly functioning. Hence the 9-level MLI which is analyzed is simulated fruitfully. In the sequential way, the results are below depicted.

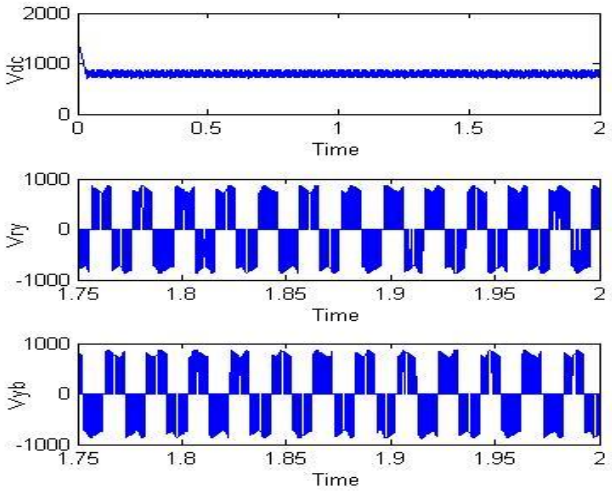

Fig.9. Voltage output of DC supply, R-Y phase and Y-B phase with conventional inverter

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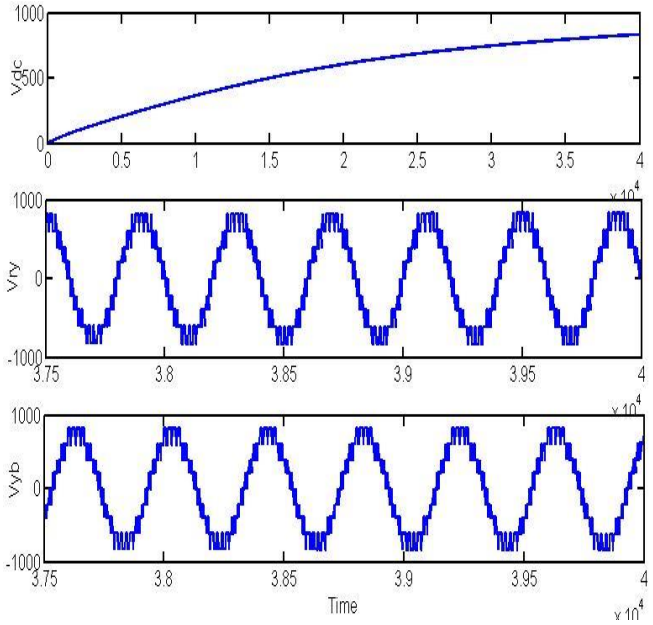

Fig.10. Voltage output of DC supply, R-Y phase and Y-B phase with 9-level ACHB MLI

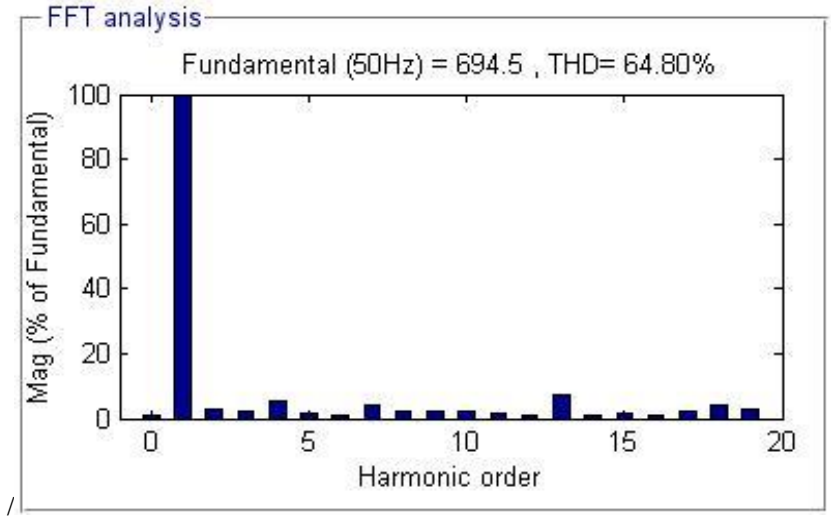

Fig.11. Harmonic analysis with conventional inverter

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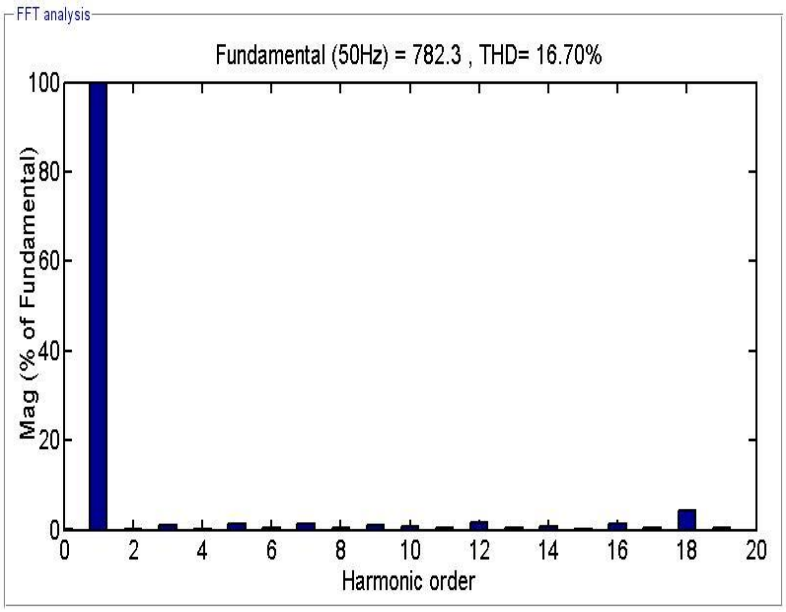

Fig.12. Harmonic analysis with 9-level ACHB MLI

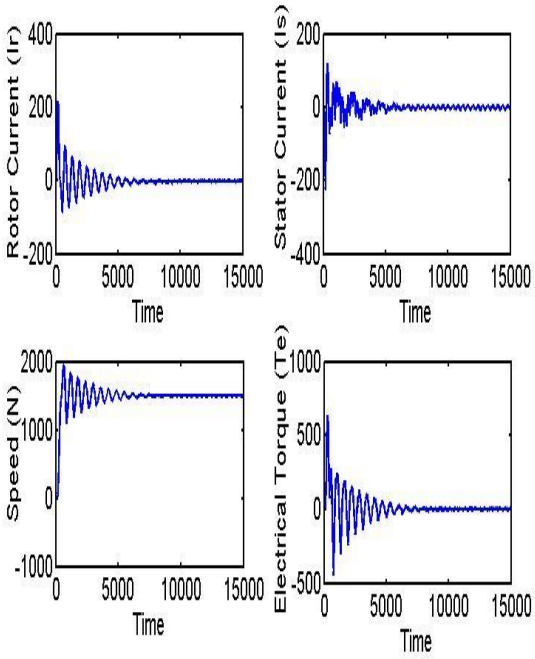

Fig.13. Various output for motor load with T= 0.1

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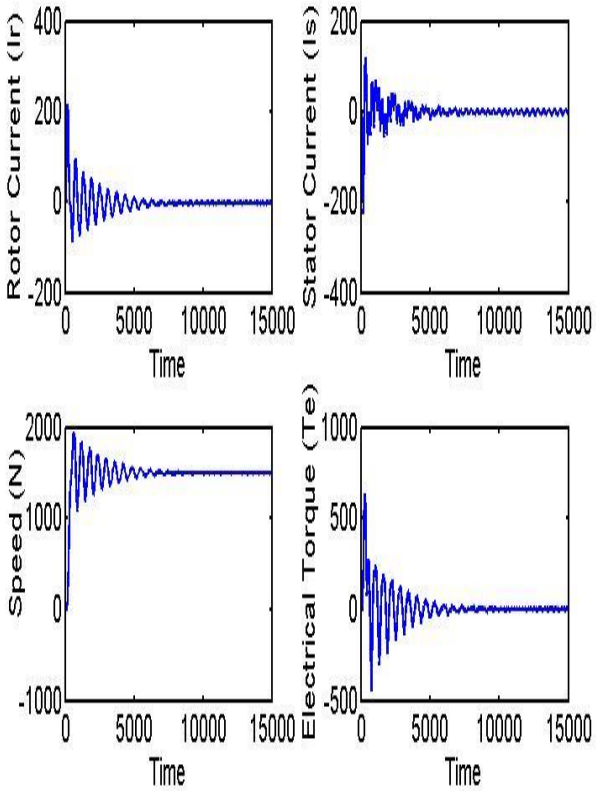

Fig.14. Various output for motor load with T= 1

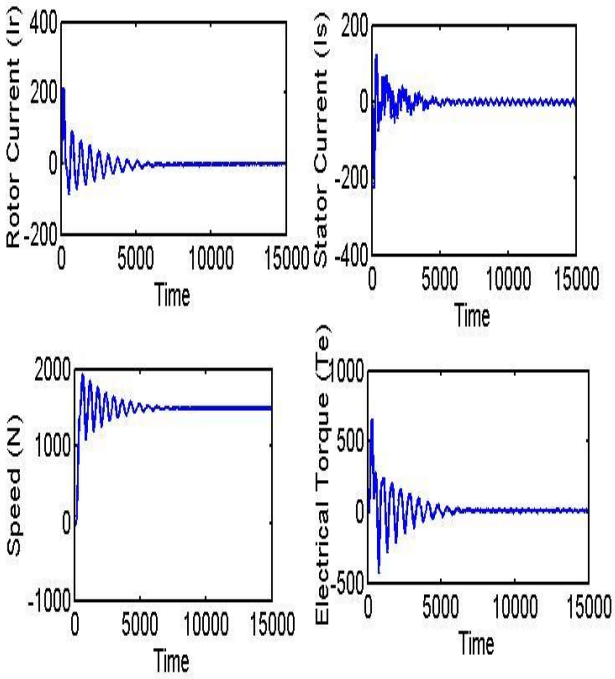

Fig.15. Various output for motor load with T= 10

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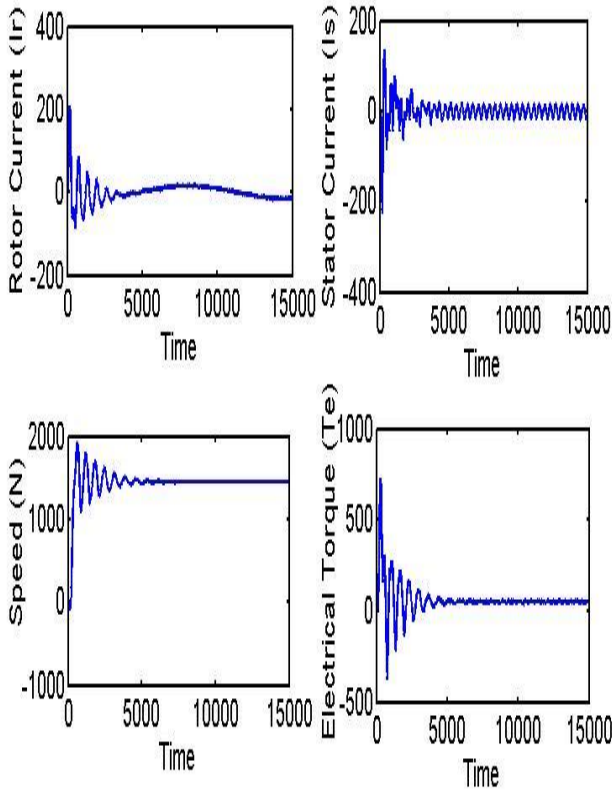

Fig.16. Various output for motor load with T= 50

Conclusion

An EMU circuit with Asymmetric Cascaded H-Bridge MLI arrangement for Railway purpose uses restricted D-C Sources have been carryout in the manuscript. Initially, multilevel inverter configuration along with switching approach was discussed. A voltage output is obtained with the implementation of Sinusoidal-PWM scheme for the reduction of unwanted harmonic contents. The analyzed MLI structure has been simulated and the results of simulation circuit are depicted. The THD % values of waveforms of voltage output are also considered. The simplicity of spreading out and redundancy in the analyzed MLI structure gives the way for increasing the amount of output levels. The MLI technique which is analyzed generates waveform of output voltage with high-quality. It can be predicted that the contour of voltage output gradually converge to reference waveform of voltage output through increasing the amount of level modules. The results of this manuscript show that the analyzed MLI configuration provides absolutely suitable results for generating the necessary waveforms.

References

1. Samir Kouro, , Mariusz Malinowski, K. Gopakumar, , Josep Pou, Leopoldo G. Franquelo, Bin Wu, Jose Rodriguez, Marcelo A. Pérez, , and Jose I. Leon, “Recent Advances and Industrial Applications of Multilevel Converters” IEEE Transactions On Industrial Electronics, Vol. 57, No. 8, August 2010.

2. N. P. Schibli, T. Nguyen, and A. C. Rufer, “A three-phase multilevel converter for high-power induction motors,” IEEE Trans. Power. Electron.,vol. 13, no. 5, pp. 978–986, Sep. 1998.

3. S. Bernet, “Recent developments for high power converter for industry and traction applications,” IEEE Trans. Power Electron., vol. 15, no. 6,pp. 1102–1117, Nov. 2000.

4. M. D. Majrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high-power applications,"IEEE Trans. Ind. Appl.., vol. 36, no. 3, pp. 834–841, May/Jun.2000.

5. Natarajan Prabaharan, Kaliannan Palanisamy, "A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications", Renewable and Sustainable Energy Reviews, Vol No.76, pp.1248-1282, April 2017.

6. J. Venkataramanaiaha, Y. Suresha, Anup Kumar Pandab, "A review on symmetric, asymmetric, hybrid and single DC sources based multilevel inverter topologies", Renewable and Sustainable Energy Reviews, Vol No.76, pp.788-812,March 2017.

7. Krishna Kumar Gupta, Alekh Ranjan, Pallavee Bhatnagar, Lalit Kumar Sahu, and Shailendra Jain, "Multilevel Inverter Topologies With Reduced Device Count: A Review", IEEE Tran. On Power Elec., Vol. 32, No. 1, pp. 135-151, January 2016.

8. Amir Taghvaie, Jafar Adabi, and Mohammad Rezanejad, "Circuit Topology and Operation of a Step-Up Multilevel Inverter With a Single DC Source", IEEE Tran. on Ind. Elec., Vol. 63, No. 11, pp.6643-6652, November 2016.

9. Emad Samadaei, Sayyed Asghar Gholamian, Abdolreza Sheikholeslami, and Jafar Adabi, "An Envelope Type (E-Type) Module: Asymmetric Multilevel Inverters With Reduced Components", IEEE Tran. on Ind. Elec., Vol. 63, No. 11, pp.7148-7156, November 2016.

10. Elyas Zamiri, Naser Vosoughi, Seyed Hossein Hosseini, Member, IEEE, Reza Barzegarkhoo, and Mehran Sabahi, "A New Cascaded Switched-Capacitor Multilevel Inverter Based on Improved Series–Parallel Conversion With Less Number of Components", IEEE Tran. on Ind. Elec., Vol. 63, No. 6, pp.3582-3594, June 2016.

11. Y. Suresh, Anup Kumar Panda, "Investigation on stacked cascade multilevel inverter by employing single-phase transformers", Engineering Science and Technology, an International Journal, Vol No.19, pp.894-903,January 2016.

12. Ye Zhan,YunWei Li, Navid R. Zargari, and Zhongyuan Cheng,"Improved Selective Harmonics Elimination Scheme With Online Harmonic Compensation for High-Power PWM Converters", IEEE Tran. On Power Elec., Vol. 30, No. 7, July 2015.

13. M. Balasubramonian and V. Rajamani, "Design and Real-Time Implementation of SHEPWM in Single-Phase Inverter Using Generalized Hopfield Neural Network", IEEE Tran. on Ind. Elec., Vol. 61, No. 11, November 2014.

14. M. S. A. Dahidah and V. G. Agelidis, "Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: A generalized formula," IEEE Trans. Power Electron., Vol. 23, No. 4, pp. 1620-1630, Jul. 2008.

15. R. M. Valan, P. S. Manoharan, and A. Ravi, "Simulation and an experimental investigation of SVPWM technique on a multilevel voltage source inverter for photovoltaic systems," International Journal of Electrical Power & Energy Systems, Vol. 52, pp. 116-131, Nov. 2013.

16. Arun Rahul S, Sumit Pramanick, R. Sudharshan Kaarthik, K. Gopakumar, and Frede Blaabjerg, "Extending the Linear Modulation Range to the Full Base Speed Using a Single DC-Link Multilevel Inverter With Capacitor-Fed H-Bridges for IM Drives", IEEE Tran. On Power Elec., Vol. 32, No. 7, pp. 5450-5458, July 2017.

International Journal of Modern Agriculture, Volume 9, No.4, 2020
ISSN: 2305-7246

17. J. Lakwal, D. M. Deshpande, A. Suresh, and A. Mittal, "Cascaded Multilevel Inverter Topologies for Photovoltaic Power Generation Systems", Int. J. of Chem. Tech. Research, vol. 5, no.2, pp. 1094-1100, April-June 2013.

18. L. Yu, H. Hoon, and A. Q. Huang, "Real-time calculation of switching angles minimizing THD for multilevel inverters with step modulation," IEEE Trans. Ind. Electron., Vol. 56, No. 2, pp. 285-293, Feb. 2009.

19. N. A. Rahim, J. Selvaraj, and C. Krismadinata, "Five-level inverter with dual reference modulation technique for grid-connected PV system," Renewable Energy, Vol. 35, No. 3, pp. 712-720, Mar. 2010.

20. N. A. Rahim, M. F. M. Elias, and H. Wooi Ping, "Transistor-clamped H-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing," IEEE Trans. Ind. Electron. , Vol. 60, No. 8, pp. 2943-2956, Aug. 2013.

21. J. Lakwal, M. Dubey, "Modelling and Simulation of a Novel Multilevel Inverter for PV System using Unequal DC Sources", 2014 IEEE International Conference on Advanced Communication Control and Computing Technologies (ICACCCT), pp. 296-300, May. 2014.