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Design and Implementation of Super Capacitor Based DVR Circuit for Power Quality Enhancement

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Abstract: Power quality complications are the sensitive issue in a power network. Two power quality issues are frequently arise in distribution structure, which are swells and voltage sag. Power quality issues affect the sensitive load. To diminish the voltage swell and sag the Dynamic Voltage Restorer (DVR) device is used.
Super-Capacitors based DVR system is suggested for mitigate the swell and voltage sag. It has the ideal characteristics like low energy density and high power for compensate the voltage sag and swell.

In this proposed super capacitor based DVR provides excessive power in a short interval of time and it is work as an energy storage. The DC-DC converter is used for integrated DVR with super capacitor. The temporary voltage sag and voltage swell is also compensated by this technique.

Keyword: Power Quality, Voltage Sag, DVR, Super Capacitor

I. Introduction

Power supply is generated by conventional and non-conventional methods. DC energy storage unit is main parts of DVR power circuits. Present time various energy storage devices are used in DVR power circuit like flywheels, batteries, SMES etc. when the DVR in operation condition it generate the real power requirements of the system [I, V].

Electrochemical capacitors are at present called by various names: super capacitor, ultra capacitor, or electrochemical twofold layer capacitor. Super Capacitor offer the chance to deliver power as required immediately. During operation, Super Capacitor creates vitality without polluting the environment, making them advantageous for a hybrid zero discharge transmission and dispersion arrange. Contrasted with the different kinds of fluid and dry batteries, Super Capacitor has an increasingly safe operation [VI-VII, X].

To satisfy the necessary electrical parameters of DVR framework, various cells must be consolidated so as to shape the supply module. As energy cradle, super capacitor is added to the DVR circuit to deliver the energy required during load operation [VIII, X].

The point of this section is to investigate the operation to replace ordinary DC energy storage for DVR power circuit with a super capacitor. Super Capacitor is an alternative energy source which is replacement of the traditional energy sources. It is proposed for DVR power circuit for various voltage sag compensation [II-IV].

II. Super Capacitor based Energy Storage (SCBES)

Super capacitor is known as ultra-capacitor. It is a very high capacity capacitor with having high capacitance as compare to normal capacitor. It is a twofold layer based capacitor; in it energy is taken care of by charge move at the breaking point among anode and electrolyte. The proportion of set aside energy is limit of electrolyte surface, the open terminal It is developed of two terminals, an electrolyte and a separator. The two anodes carbon give a high surface area part. In the super capacitor no chemical reaction, the energy storage in the electrostatically. Super capacitor is a double layer. To design a multiple electric charge in the super capacitor, it is used the materials which having high surface area [II-IV,

IX, XI -XIII]. Super capacitor based energy storage system is integrated with the battery.

III. Modelling of a Super Capacitor System

Super Capacitors are developing as one of future alternative energy resource to replace conventional energy sources and produce DC voltage yield**.**

Super capacitors can be categories into three types

1) Hybrid capacitors
2) Pseudo capacitors
3) Double-layer capacitors

For the important task like power fluctuation mitigation by means of releasing the real power and charging, which may be required on account of pinnacle request, transient blemish and different reasons and smoothing of voltage can be achieved by using the Super capacitor Based Energy Storage System.

$V_c = Q/C$
$E = (½)*C*V^2$
Q = Stored Charge
C = Super capacitor (Capacitance)

Super capacitors execution incorporates the different details: evaluated current, working DC voltage, spillage current, explicit force, explicit vitality, capacitance resilience, capacitance run and a level of absolute capacitance and proportional arrangement obstruction (ESR). Working DC voltage (WVDC).

Table: 1.1 Properties Comparison of Flywheel, Super Capacitor and Battery

Properties	Super Capacitor	Flywheel	Battery
Efficiency (η)	> 94%	78-94%	79-87%
Discharge Time	1to 30 s	0.5 o 2 h	0.3 to 3 h
Safety	Good	Not Good	Good
Charge Time	1to 30 s	0.5 to 2 s	1to 5h
Energy Density	1 ‹ ED ‹ 10	5 ‹ ED ‹ 50	20 ‹ ED ‹ 100
Maintenance	Very Good	Medium	Good
Power Density (Wh/kg)	7500~ 18500	170~ 1900	60~ 250
Cycle life	More than 10^6 times	Around 10^6 times	Around 10^3 times

If P stored ≥ P rated i.e. the super capacitors voltage Usc will drop to 0 V in the event that all the put away vitality is used, at that point the limitation appraised power yield ability would be abused. Subsequently a lower limit is fixed on the super capacitors voltage Umin, is 50 % of Umax, with the goal that 75% of put away vitality can be used proficiently.

Since the voltage pace of super capacitors cell is low in this way the super capacitors bank would comprise of number of super capacitors cells in arrangement and equal with the goal that the necessary voltage level and adequate valuable vitality can be put away.

Stern and Tafel equation is given for the super capacitor:

$$V = \frac{NN_S Qx_2}{N_P N^2 \varepsilon\varepsilon_O A} + \frac{NN_S 2RT}{F} \alpha r \sinh\left[\frac{Q}{N_P N^2 A\sqrt{8RT\varepsilon\varepsilon_O c}}\right] \qquad -i_c(t) = Ai_o \exp\left[\frac{\alpha F\left[\frac{V}{N_s} - \frac{V_{\max}}{N_s} - \Delta V\right]}{RT}\right] N$$

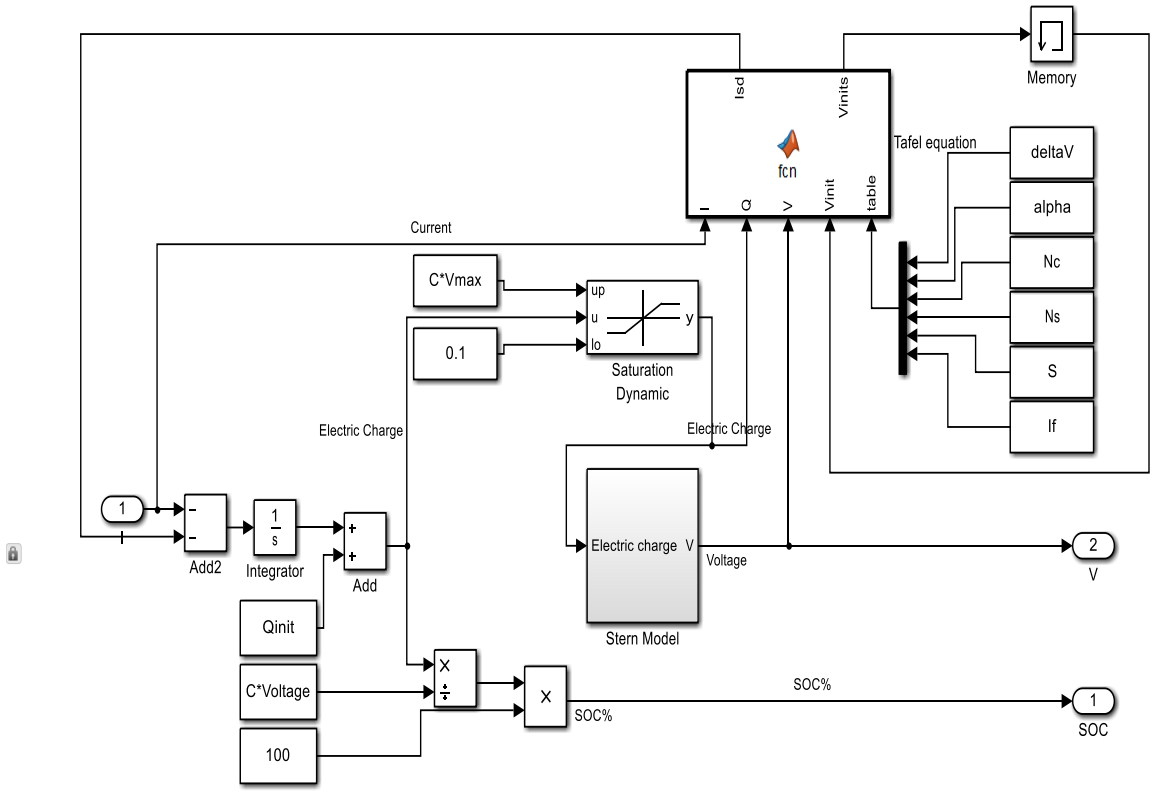

Fig.1: Internal Parameters Model Structure of Super Capacitor

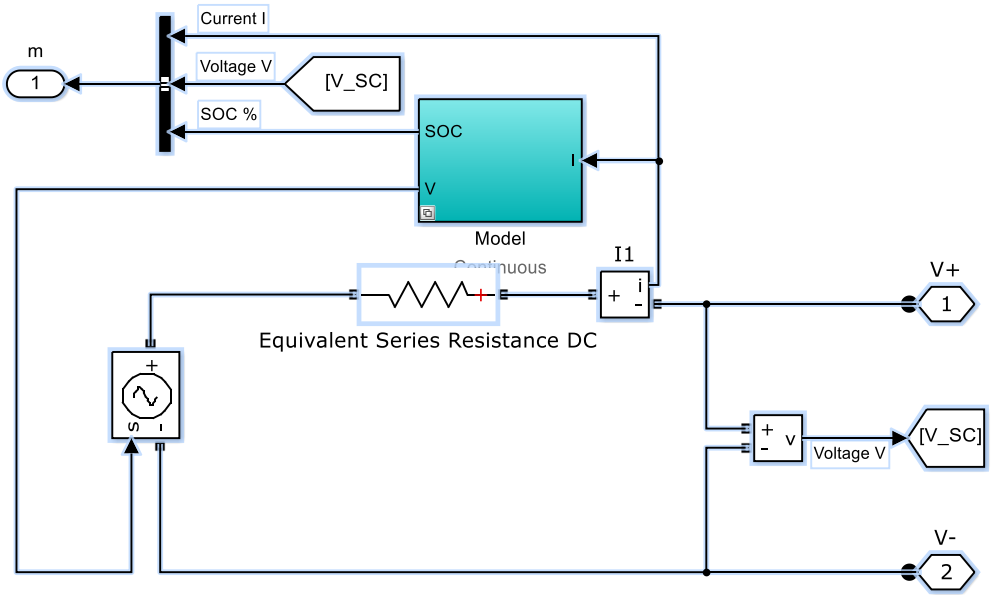

Fig. 2: Identical Circuit Model of Super Capacitor Based Energy Storage System

IV. Calculation of Size of Super Capacitor Bank

The super capacitor bank Maximum energy storage is calculated by
$E_{max} = (C_{eq} \times U^2_{max})$
Where:
E_{max} = Maximum energy storage capacity
U_{max} = Super capacitor maximum voltage
C_{eq} = Super capacitor equivalent capacitance bank (Farad)
The super capacitor bank voltage discharge ratio is given by
$\% d = [\{U_{max}\}/\{U_{min}\}] \times 100$
Where;
U_{min} = Super Capacitor voltage boundary (minimum allowable)
The maximum power of the super capacitor bank can be calculated by:
$P_{Dmax} = [U^2_{max}]/[4R_{eq}]$
Where:
P_{Dmax}= Power KW (maximum dischargeable)
R_{eq} = super capacitor bank equivalent series resistance

$E_u = C_{eq}[(U_{max} - U_{min})^2]$ is provided when $U_{min} < U < U_{max}$

V. Calculation of Capacitance in Super Capacitor Bank

The Super capacitor equivalent capacitance is given by:
$C_{eq} = (N_p \times C_{cell}) / N_S$

For higher energy storage capacity $Np > N_s$

Number of series connected cells (Ns) = U_{max}/U_{cell}

The super capacitor bank parallel branch N_p is given calculated as :

$$N_p = (N_s \times C_{eq})/C_{cell}$$

The number of cell in the super capacitor bank is equal to N_{Total}

$$N_{Total} = N_{Parallel} \times N_{series}$$

VI. Calculation of Series Resistance in Super Capacitor Bank

ESR is comprise of terminal opposition, electrolyte obstruction and contact opposition that waste force causes inner warming while charging or releasing in super capacitor. ESR is practically short of what one million yet impacts the vitality effectiveness and force thickness. While structuring the super capacitor cells are associated in arrangement and equal in this way complete arrangement opposition of the bank, which is spoken to by following equation:

$$R_{eq} = (R_s \times N_S)/ N_P$$

Parallel arms should always higher than N_S thereby lower ohmic losses in the super capacitor bank while charging and discharging.

VII. Advantage and Disadvantage of Super Capacitor

The most extreme necessity of legitimate plan and execution of SCES is keeping up the unwavering quality of the transmission of intensity circulation framework in the lattice accomplice method, the exchanging transient method, the island method. This is additionally significant in different investigations, for example, supported interferences, voltage glimmer, voltage lists, sounds, voltage guideline, voltage strength.Some of the advantages and disadvantages are explained as below.

Advantages of Super Capacitor

Super Capacitor has following advantages

1. It follow boundless cycle
2. It is never overcharge and full charge cut of circuit is not required.
3. Charging time is very fast.
4. It has low impedance it is effect enable high current
5. It has Cost effective storage and power applications.
6. It has high efficiency.
7. It is minimal, lightweight and has no moving parts. In this way it is 99.9% dependable.
8. It has most minimal contamination rate when contrasted with batteries just as fuel controlled gadgets. Thus, pollution is reduced by 99%.
9. The overall efficiency of a Super Capacitor is high as compared to battery.
10. The reason for using Super Capacitor is that it does not need produce noise, hurtful discharge or dirtying gases and it is without fuel. Such a measured Super Capacitor framework can be immediately introduced anyplace, requires negligible upkeep to keep the framework running and furthermore no moving parts to wear out or separate.

Disadvantages of Super Capacitor

1. To achieve higher voltages from low voltage cells, a combinations are required
2. It is holds 0.2 – 0.1 low energy thickness of a battery.
3. In the some applications the full energy range cannot be utilized

VIII. Super Capacitor Based DVR Test Systems

Electrical circuit model of Super Capacitor Based DVR is presented in Fig.3. The power system circuit is integrated with generator (11 kV, 50 Hz) & three phase transformer of star/delta/delta (11/132/11 kV). Table 2 shows the detailed system parameters.

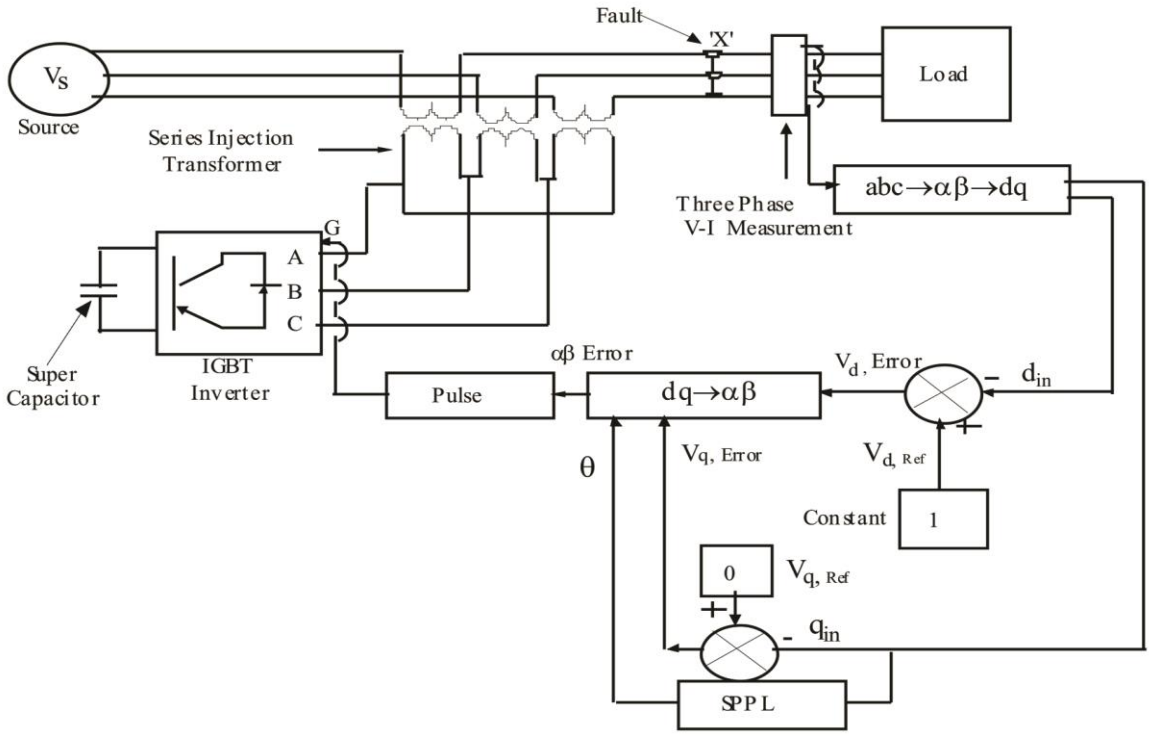

Fig. 3: A Super Capacitor based DVR Model

Table 2: Super Capacitor Based DVR System Circuit Parameters

Items	Values
Transmission Line Length	6 km
Inverter Significance	6 Pulse, IGBT based, Sample Time = 5 μs Carrier Frequency =1080 Hz, 3 arms
Capacitor	750×10^{-6} F
Parameters of Transmission Line (T.L.)	Inductance = 0.94 (mH/km) Capacitance = 13 (nF/km) Resistance = 0.012 (ohms/km)
Load	R = 0.12 ohms, L = 0.19 H

IX. Compensation of Sags with Super Capacitor Based DVR System for Power Quality Enhancement

A DVR design which incorporates a Super Capacitor based DVR module as a DC voltage source is tested for PQ improvement and it is analysed for symmetrical and unsymmetrical voltage sag compensate using MATLAB/Simulink. In the various cases of voltage sag compensation impact of super capacitors are analysed.

Case 1: Three Phase Fault at 11 kV Distribution Line

Performance of Super Capacitor based DVR is analysed on 11Kv distribution line by generating the three phase fault. A three phase fault is generated at time of 0.4 s, the time period of fault is taken for 0.2s i.e fault from 0.4 to 0.6. The amount of sag is consider 26 percent and voltage drop is considered 0.26 p.u. To compensate this sag, the voltage is required 0.26 p.u. from Super Capacitor based DVR to mitigate the fault. Analysis of positive, negative and zero sequence component of three phase fault with or without Super Capacitor based DVR as shown in Fig.4.

Fig.4 shows the rated 11 kV voltage is achieved in presence of the Super Capacitor based DVR parameters as shown in Table 3 and it is observed that for the three phases balance condition the negative sequence is always zero. The DC energy storage capacity is 4366kV is required from super energy storage for this compensation.

Table 3: Super Capacitor Parameters-I

Items	**Values**
Capacitance Rated	500(F)
Equivalent DC Series resistance	$2.1e^{-3}$(ohms)
Series Capacitors	2182 No.
Parallel Capacitors	200 No.
Rated Voltage (V)	2V
Surge Voltage (V)	2.1V
Operating temperatures	25°C(Celsius)
No. of Layers	6
Initial Voltage	2V
Leakage Current	$5.2e^{-3}$A
Charge Current	10.2 A

Time	1988 second
Molecular Radius	$1.23e^{-9}$ (m)
Over Potential	0.3V
α	0.3

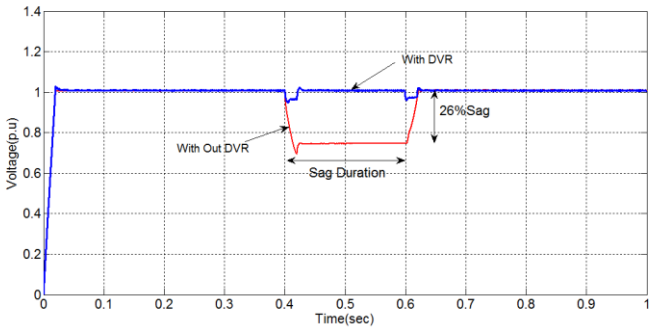

Fig.4: Analysis of three Fault with or without Super Capacitor based DVR

Case 2: Analysis of Single- Line -to Ground Fault (LLG) for Distribution Line of 11kV

For analysis SLG fault at the 11Kv distribution line and performance of Super Capacitor based DVR is analysed by MATLAB/Simulink.

A SLG fault is generated at time of 0.4 s, the time period of fault is taken for 0.2s i.e fault from 0.4 to 0.6. The amount of sag is considered 17.02 percent and voltage drop is considered 0.1702 p.u. (11 kV=1p.u.). Analysis of positive, negative and zero sequence component of SLG Fault with or without Super Capacitor based DVR as shown in Fig.5.

Table 4: Super Capacitor Parameters-II

Items	**Values**
Capacitance Rated	500(F)
Equivalent DC Series resistance	$2.1e^{-3}$(ohms)
Series Capacitors	1881 No.
Parallel Capacitors	170 No.
Rated Voltage (V)	2V
Surge Voltage (V)	2.1V
Operating temperatures	25°C(Celsius)
No. of Layers	6
Initial Voltage	2V
Leakage Current	$5.2e^{-3}$A
Charge Current	10.2 A
Time	1988 second
Molecular Radius	$1.23e^{-9}$ (m)
Over Potential	0.3V
α	0.3

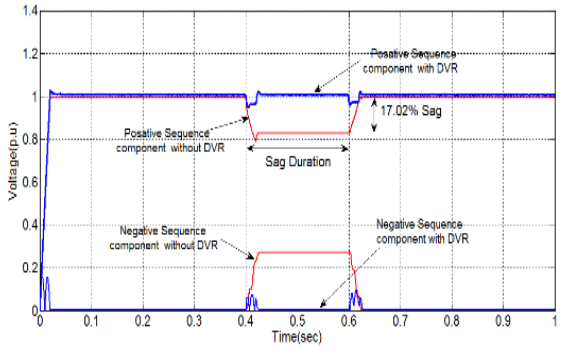

Fig.5: Analysis of SLG Fault with or without Super Capacitor based DVR

The desired voltages are injected by Super Capacitor based DVR using the space vector PWM inverter and control technique. In Fig.5 it is observed that the rated (11 kV=1p.u.) voltage is achieved in presence of the Super Capacitor Based (DVR)parameters as shown in Table 4 and it is also observed that in the presence of Super Capacitor based DVR negative sequence component is nearly zero as shown in Fig.5. The DC energy storage capacity is 3766kV is required from super energy storage for this compensation.

Case 3: Analysis of Double- Line -to Ground Fault (LLG) for Distribution Line of 11kV

For analysis SLG fault at the 11Kv distribution line and performance of Super Capacitor based DVR is analysed by MATLAB/Simulink.

A LLG fault is generated at time of 0.4 s, the time period of fault is taken for 0.2s i.e fault from 0.4 to 0.6. The amount of sag is considered 17.02 percent and voltage drop is considered 0.1702 p.u. (11 kV=1p.u.). Analysis of positive, negative and zero sequence component of LLG Fault with or without Super Capacitor based DVR as shown in Fig.6

Table 5: Super Capacitor Parameters-III

Items	Values
Capacitance Rated	500(F)
Equivalent DC Series resistance	$2.1e^{-3}$(ohms)
Series Capacitors	1881No.
Parallel Capacitors	170 No.
Rated Voltage (V)	2V
Surge Voltage (V)	2.1V
Operating temperatures	25°C(Celsius)
No. of Layers	6
Initial Voltage	2V
Leakage Current	$5.2e^{-3}$A
Charge Current	10.2 A
Time	1988 second
Molecular Radius	$1.23e^{-9}$ (m)
Over Potential	0.3V
α	0.3

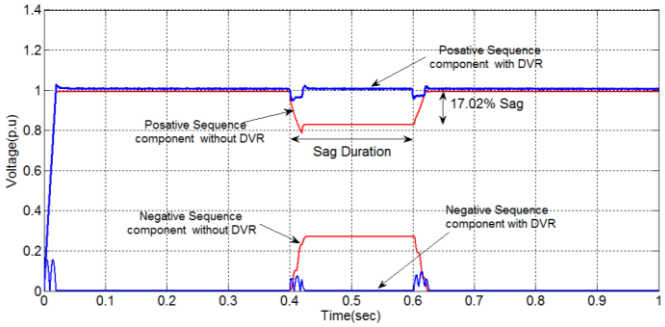

Fig.6: Analysis of LLG Fault with or without Super Capacitor based DVR

The desired voltages are injected by Super Capacitor based DVR using the space vector PWM inverter and control technique. In Fig.6 it is observed that the rated (11 kV=1p.u.) voltage is achieved in presence of the Super Capacitor based DVR parameters as shown in Table 5 and it is also observed that in the presence of Super Capacitor based DVR negative sequence component nearly zero as shown in Fig.6. The DC energy storage capacity is 3766kV is required from super energy storage for this compensation.

Case 4: Line to Line (LL) Fault at 11 kV Distribution Line

For analysis three phase fault at the 11Kv distribution line and performance of Super capacitor based DVR is analysed by MATLAB/Simulink.

A LL fault is generated at time of 0.4 s, the time period of fault is taken for 0.2s i.e fault from 0.4 to 0.6. The amount of sag is consider 26 percent and voltage drop is considered 0.26 p.u. Analysis of positive, negative and zero sequence component of LL Fault with or without Super Capacitor based DVR is presented in the Fig.7.
Fig.7. is presented that the pre sag voltage 11 kV is acquire in existence of the Super Capacitor Based (DVR) parameters as shown in Table 6 and it is also observed that in the presence of Super Capacitor based DVR negative sequence component is nearly zero as shown in Fig.7. The DC energy storage capacity is 4366kV is required from super energy storage for this compensation.

Table 6: Super Capacitor Parameters-IV

Items	Values
Capacitance Rated	500(F)
Equivalent DC Series resistance	$2.1e^{-3}$(ohms)
Series Capacitors	2182 No.
Parallel Capacitors	200 No.
Rated Voltage (V)	2V
Surge Voltage (V)	2.1V
Operating temperatures	25°C(Celsius)
No. of Layers	6
Initial Voltage	2V
Leakage Current	$5.2e^{-3}$A
Charge Current	10.2 A
Time	1988 second
Molecular Radius	$1.23e^{-9}$ (m)

Over Potential	0.3V
α	0.3

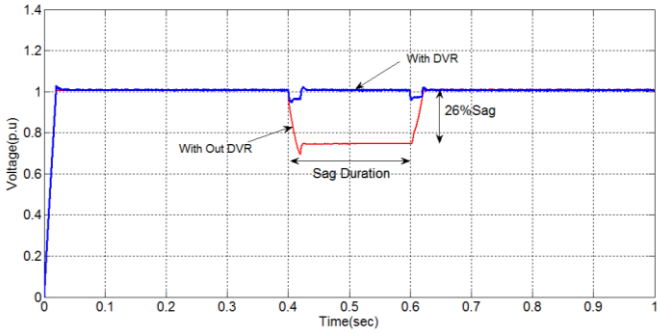

Fig.7: Analysis of Capacitor based DVR for LL Fault

Conclusion

The functional behaviour of the super capacitor is explained briefly to allow a specific operation of this novel possibility of power supply and its peculiarities in combination with a DVR applied for voltage sag compensation in distribution system. Some of the advantages and disadvantage Super Capacitor are discussed in this paper.

Super Capacitor based DVR module is introduced in the DVR power circuit which is equal to DC voltage source, which is replacement of conventional energy source like battery, SMES and flywheel. The new proposed has been simulated on various symmetrical (3-phase fault) as well as unsymmetrical fault (SLG, LL and LLG) conditions. It is observed, proposed method can correctly compensate the voltage sag with high degree of accuracy and reliability. The Super Capacitor based DVR has capacity for mitigation of symmetrical and unsymmetrical fault. As a result super capacitor cells can offer a viable alternative to batteries.
A Super Capacitor Based DVR is implemented to mitigate various symmetrical as well as unsymmetrical fault conditions. Advantages and disadvantages for implementation of Super Capacitor are also discussed.

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