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Design and Verification of Asynchronous FIFO

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***Abstract*—**The major issue in transferring a data from one clock domain to another clock domain is synchronization and data loss which affects the performance and data transfer speed. To overcome this, asynchronous FIFO's are implemented using gray codes and dual flip-flop synchronizers. In this proposed technique, it consumes low power and ensures safe transmission of data. Transistor count, power dissipation and delay are minimized and speed is increased. RTL Verilog coding is used. It is observed that the power will be reduced to half of its value. By using the Asynchronous FIFO designed using gray pointer and dual flip-flop we can transmit the data safely with no data loss and we can further reduce the power, area and delay. Performance, efficiency and speed also gets increased. This can be implemented using Verilog coding and simulated in Xilinx tool. It verified in real time using Spartan-6 FPGA kit.

Keywords-*FIFO;FPGA;RTL;Verilog;Testbench;DFT*

I. INTRODUCTION

The basic building block of data transmission is synchronization. Synchronization may be achieved by using a Flip-flop as a synchronizer by giving the data generated in the source clock as input to the Flip-flop and using destination clock as driving clock. A Flip-flop is made up of many gates. It is the speed and lossless data transmission we are concerned about. The data transmission can be improved by using various techniques. Speed, power and chip area are the most often used measures to find efficiency of an algorithm, there is a strong link between the algorithms and technology used for the implementation.

Synchronizers and gray codes plays an important role in today's Very Large Scale Integration and various other applications. Earlier, the major challenge for VLSI designer was to reduce area of chip by using efficient optimization techniques to satisfy MOORE'S law. Then the next phase is to increase the speed of operation to achieve fast calculations like, in today's microprocessors millions of instructions are performed per second. The clear understanding of the asynchronous FIFO is to synchronize the clock frequency between two control signals that define the performance-based test requirements as well as safety steps[6]. Many researchers have tried and are trying to design asynchronous data transmission with advancements in technology that give any of the following design targets: high speed, low power consumption, layout regularity and thus less region.

The common data transfer method between two clock regions is using a Flip-flop as a

synchronizer. In asynchronous data transfer, clock speeds of the regions are the main parameter that determines the performance of the data transfer. By the use of increased Flip-flops, the synchronization can be done better which may give rise to reduction speed. Due to irregularity of structure, silicon area increases and due to the increase in interconnect resulting from complex routing, power consumption also increases.

Asynchronous FIFO technique is used for low power and high speed data transfer .It uses dual Flip-flop and gray code pointers .It enables low power and high speed digital circuits. An efficient FIFO should transfer data without loss and it should perform operation at high speed, different clock domains. It should occupy less number of slices and LUTs and consume less power. The FIFO must indicate that it is full or empty. Data transfer has three main steps- write, read and synchronization.

In an Asynchronous FIFO data is transferred between two different clock domains by using pointers working in that clock domain. Simultaneously, the pointers are synchronized in the opposite clock domains instead of synchronizing the data. In the case of OFDM or SCFDMA, by simply instantiating more units that process multiple subcarriers in parallel, the throughput can be increased[7]. The pointers generated in one clock domain is converted to the gray code and the synchronized in the another clock domain to avoid damage. As clock speed highly varies the data loss is very high. It comes under normal data transfer. In asynchronous FIFO, data loss is reduced. But, the data transfer speed is increased.Data transfer is based on the read and write operations. The data is written in the FIFO first and then read[3].

In the section 1, a detailed description of the asynchronous data transfer is given. In the section 2, various asynchronous data transfer methods and their differences are mentioned. In the section 3, data transfer using asynchronous FIFO, simulation results of the proposed system and the specification of the FPGA used for verification are discussed.

II. RELATED WORK

A Flip-flop used as synchronizer is used to synchronize the data in the destination clock domain. The synchronizer is designed and implemented using 180nm CMOS process technology. The proposed system provides a good compromise between cost and performance in asynchronous data transfer. The proposed asynchronous FIFO for low power and high performance neural network training circuits has been implemented using gray code pointers The hardware includes dual Flip-flops for synchronizing the pointers.

A. Flip flop synchronizers

The Flip-flop (single, dual or triple) is a hardware synchronizer design. But, it is very slower and causes huge data loss in asynchronous data transfer. Flip-flop synchronizers attempt to synchronize the data in the receiver clock. But, increases the delay and reduces the data transfer speed. Because of this, Flip-flop synchronizers have a less expensive. But, increases the data loss during data transfer between large different clock speeds. In this data loss is reduced by transmitting the data based on the receiver speed or receiving the data based on the transmitter speed. But, both decreases the data transfer speed, performance and increases the power consumption. This method leads to high data loss and power consumption [2].

B. Handshake Mechanisms

Handshake based data transfer mechanism is another way to transfer the data between two clock domains. This mechanism works as there is a synchronization between the sender and receiver to avoid data loss. The data is transmitted safely by synchronizing the transfer information. This achieves the safe transfer of the data. But, results in large delay which reduces the transfer speed and rate. Due to this mechanism the data loss is reduced. But, it also reduces the transfer rate. Because, the synchronization mechanism requires control bits and error control mechanisms which increases the transistor count and reduces the performance and speed.

The above both mechanisms are transfer the data safely and reduces the data loss. But, they reduces the speed and transfer rate. It reduces the system performance. Because, for fast calculation and high performance the data transfer must have high speed and rate. They also produces high delay which also affects the system performance. For high speed computations the data transfer speed must high and must not have any data loss. But, using above methods the data rate is limited which also limits the system performance. To increase the system performance the data rate must be high. High performance system can be achieved by increasing the data transfer speed. The data transfer speed is increased by using the asynchronous FIFO described in this paper.

The objective of this paper is to design an asynchronous FIFO and its DFT (Design for verification) to verify the FIFO in real time. The DFT is used for only verification purpose. It used to generate the data and control signals needed by the design. Testbench and DFT used for the verification can. Verification is used to find the errors and bugs in the design.

By using deep verification a design with low errors or with no errors can be released. The verification proposed by this paper is done using the test bench and DFT.

The asynchronous FIFO ensures the safe transfer of data between two independent clock domains. It ensures high transfer speed and lossless transmission. The size of the FIFO is based on the clock speeds and the functional requirements like speed of the transmission. This paper compares the performance of data transfer protocols time needed to compete the data transfer. The synchronizer based data transfer has the high delay and data loss. The handshake mechanism can reduce the data loss. But, it needs careful design and many control signals. Finally the asynchronous FIFO is the best method to transfer the data between independent clock domains

III. ASYNCHRONOUS FIFO

In Handshake based data transfer protocols the control signals are used for data transmission. Further optimization in area, power and delay has been done. The aim of our project is to design a low power, low complexity and high speed data transfer using asynchronous FIFO. There are several disadvantages in the existing data transfer mechanism. Many units are reduced and safe data transfer is achieved. It can transfer the data between any clock domains. The data transfer speed is limited by only the source and destination clock speeds. There are two types of asynchronous FIFO pointers, they are read pointer and write pointers [4].

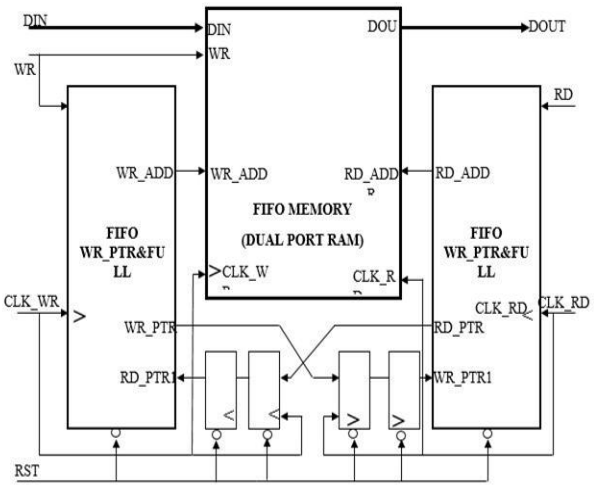

Fig. 1 Asynchronous FIFO

In the proposed system, Asynchronous FIFO based data transfer mechanism is used to transfer the data between independent clock domains. It can be used for high speed and low power data transmissions. It enables low power and high speed digital circuits. This mechanism can be used for any digital circuit needs safe and high speed data transfer like high speed microprocessors, mobile IP's and wireless data transfer mechanisms. It can be used in any digital systems.

Thus the transistor count, area, power dissipation and delay is minimized. Speed is increased. The program for the Asynchronous FIFO, Testbench and DFT is written using RTL Verilog coding, Xilinx tool is used for implementation and delay, transistor count, power consumption is measured. It is compared with the existing system and the performance is calculated.

The proposed multiplier is simulated using Xilinx ISE 14.7 and the following results are obtained and it is compared with the existing system. The ISim simulator of Xilinx is used for the simulation. The Xilinx XST tool is used the synthesize. Spartan 6 XC6SLX16-FTG256 FPGA board is used for the real time verification. An internal signal (last operation) is used to identify the condition of FIFO(full or empty)[5].

The design is verified using various clock speed for the read and write operations. The maximum clock speed used is 25Mhz which is builtin in the FPGA board. The full and empty signals are enabled properly and the reset is working very well. The system is verified using both RTL verification and FPGA verification[1].

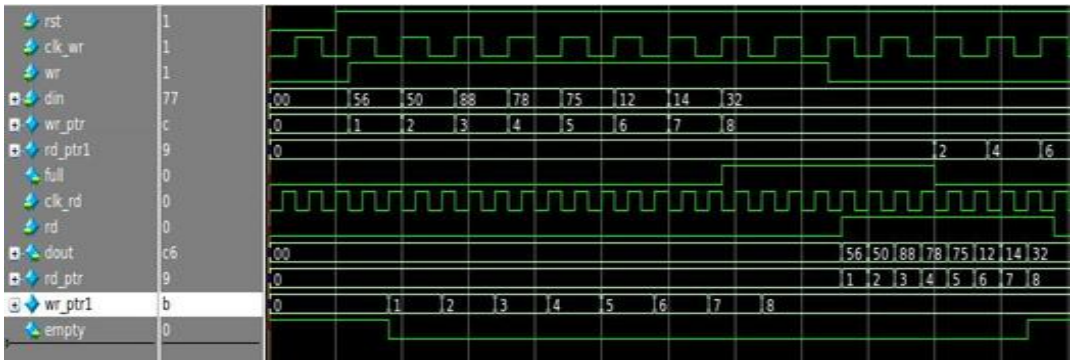

Fig. 2 Simulation output of Asynchronous FIFO

TABLE 1 FPGA DETAILS

Property Name	Value
Family	Spartan 6
Device	XC6SLX16
Package	FTG256
Speed	-5
Top-Level source type	HDL
Synthesis Tool	XST(Verilog/VHDL)
Simulator	Isim(Verilog/VHDL)
Preferred language	Verilog
Enhanced design summary	Enabled
Property Specification in project file	Store all values

IV. CONCLUSION

In the existing system, power consumption, performance, area, delay, speed and efficiency are the main drawbacks. Hence, to overcome the drawbacks, proposed system is designed by using the dual Flip-flop synchronizers.. In the proposed system, an efficient high speed and low power consumption asynchronous data transfer is designed using the asynchronous FIFO which is implemented using pointers and synchronizers to safely cross the clock domains. Thus the performance, efficiency and speed gets increased. Thus the asynchronous data transfer is very easy to achieve the high data transfer speed and secure data transfer.

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